REMARKS

Claims 1- 2, 5 - 6, 9 - 10, 12, 14 - 19, and 23 - 26 are pending. Claims 3, 4, 7, 8, 11, 13, 20 - 22 have been cancelled without prejudice. Claims 23 - 27 have been added. Claims 1 and 5 have been amended.

In response to the restriction requirement set forth in the August 20, 2002 Office Action, applicants confirm the election of Group 1, which is the species of Fig. 1. Pending claims 1 - 2, 5, 6, 9 - 10, 12, and 14 - 19 read on the species of Fig. 1. Claims 3, 4, 7, 8, 11, 13, 20 - 22 have been cancelled without prejudice.

The Examiner objected to the drawings under 37 C.F.R. § 1.83(a). The Examiner rejected claims 5 - 6 and 22 under 35 U.S.C. § 112, first paragraph, as containing subject matter not described in the specification. The Examiner rejected claims 1, 5, 21, and 22, under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 5,747,837 to Iwase et al. (the Iwase reference) in view of the Applicant Admitted Prior Art (AAPA). The Examiner rejected claims 2 and 6 under 35 U.S.C. § 103(a) as being obvious over the Iwase reference and further in view of the U.S. Patent No. 5,477,413 to Watt (the Watt reference.) The Examiner rejected claims 9 and 15 - 18 under 35 U.S.C. § 103(a) as being obvious over U.S. Patent No. 3,955,210 to Bhatia et al. (the Bhatia reference.) The Examiner rejected claims 10, 12, and 19 under 35 U.S.C. § 103(a) as being obvious over the Bhatia reference and in view of the AAPA. The Examiner rejected claim 14 under 35 U.S.C. § 103(a) as being obvious over the Bhatia reference in view of the Iwase reference and further in view of the Watt reference. These rejections are respectfully traversed.

In response to the Examiner's objection under C.F.R. 1.83(a), please note that

claim 22 has been cancelled without prejudice. However, independent claim 5, as amended, includes a feature of a semiconductor substrate serving as a base. This feature is supported by the drawing as follows. The base of the transistor is illustrated residing in the p well 20 of Fig. 1. The p well 20 and the semiconductor substrate 10 are both of the p conductivity type and are therefore electrically connected. Therefore, the semiconductor substrate can serve as a base for the second lateral bipolar transistor.

As mentioned above, Fig. 1 supports the claiming of a portion of said semiconductor substrate serving as a base of a second lateral bipolar transistor. The specification also supports the use of a portion of said semiconductor substrate serving as a base of a second lateral bipolar transistor. Specifically, on page 18, lines 21 - 24, it is disclosed that the well regions 20, 20a, and 20b may be omitted and the base BS region of the transistor NB may be made of a portion of the substrate 10. Fig. 4 is a plan view of Fig. 1, so it follows that in Fig. 1, the well region 20 may be omitted and a portion of said semiconductor substrate may serve as a base of the second lateral bipolar transistor. Therefore, applicants respectfully submit that claims 5 and 6 meet the requirements of 35 U.S.C. § 112, first paragraph.

The present invention is directed to an input protection circuit for an integrated circuit device. The input protection circuit protects the circuit from electrostatic discharge (ESD). A lateral PNP transistor PB and a lateral NPN transistor NB are serially connected between an input terminal and a reference potential. Within the PB transistor a PN junction diode D1 is formed. In the NB transistor, a PN junction diode D3 is formed. If a positive bias large ESD voltage is input, the transistor NB turns on. If

a negative bias large ESD voltage is input, the transistor PB turns on.

Claim 1, as amended, recites:

An input protection circuit comprising:

an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate;

third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate; and

a circuit formed in said semiconductor substrate and connected to said input terminal;

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, said first lateral bipolar transistor

operating without a fixed base bias, and said fourth well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

The Iwase reference relates to a semiconductor device having an input protection function. A CMOS inverter circuit 14 is connected to a semiconductor device 10. The circuit 14 receives power from the power supply V_{cc} and ground V_{ss}. The circuit operates in response to an input signal IN input through an input terminal 13 of the semiconductor device 10. An n^- type well region 16 is defined in the p^+ type semiconductor substrate 11. First 17 and second 18 p^+ type diffusion regions and an n^- type diffusion region 19 for a contact are defined on part of the surface of the n-type well region 16 in the lateral direction. A lateral pnp transistor 20 is formed by using the first p^+ type diffusion region 17 as a collector, the second p^+ type diffusion region as an emitter, and the n^- type well region as the base. *Col. 3, line 52 - col. 4, line 17; Fig. 1.*

The first p^- type diffusion region 17 is connected to ground V_{ss}. The second type p^+ type diffusion region is connected to the input resistance through the parasitic resistance R_i. The n- type diffusion region 19 is connected to a third power supply V_{pp} having a voltage higher than that of the high-potential power supply V_{cc}. With this device arrangement and connections, the PN junction between the n^- type well region and the first p^+ type diffusion region 17 is reverse biased. A p^- type well region is defined on another part of the surface of the n^- type well region 16. A lateral npn transistor 26 is formed by using the first n^- region 23 as a collector, the second n^- region as an emitter, and the p^- type well region 22 as the base. The first n^- diffusion region 24 is connected to the input terminal via 13 through parasitic resistance r1. The p^+ type diffusion region 25 is connected to a four power supply V_{BB} having a voltage lower than

that of ground V_{ss}. In a representative embodiment, the voltage of the third power supply V_{pp} is set to 5.0 volts and the fourth power supply is set to -1.5 volts. *Col. 4, line 18 - 45.* The voltage V_{pp} is applied to the n^- type well region 16 (base) of the lateral pnp transistor 20. *Col. 4, lines 50 - 5; Fig. 1.*

The Iwase reference does not disclose, teach, or suggest the circuit in claim 1, as amended. Unlike the circuit in claim 1, as amended, the Iwase reference does not disclose an input protection circuit including an input terminal for supplying an input signal to a circuit to be protected; a semiconductor substrate of a first conductivity type; a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate; first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base; a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate; third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate; and a circuit formed in said semiconductor substrate and connected to said input terminal; wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, *said first lateral bipolar transistor operating without a fixed base bias*, and said fourth well region and

the base of the second lateral bipolar transistor are connected to one reference potential node.

In contrast, the Iwase reference discloses that the first lateral bipolar transistor operates with a fixed base bias because the base of first lateral bipolar transistor, i.e., n^- type well region 16, is supplied with a known constant operating voltage V_{pp} (e.g., 5 volts). *Col. 4, lines 7 - 27 and 50 - 54.* This is not the same as an input protection circuit including a first lateral bipolar transistor with a portion of said first well region serving as a base, *said first lateral bipolar transistor operating without a fixed base bias* because the base of the first lateral bipolar transistor of the Iwase reference operates with a fixed base bias. Accordingly, applicants respectfully submit that claim 1, as amended, distinguishes over the Iwase reference.

Claim 1, as amended, further distinguishes over the Iwase reference. Unlike the circuit of claim 1, as amended, the Iwase reference does not disclose an input protection circuit including a second impurity doped region, a first lateral bipolar transistor, and a third well region, *said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region.*

In contrast, the base of said first lateral bipolar transistor of the Iwase reference is connected to a voltage V_{pp} and is not connected to the second impurity doped region or the third well region. *Col. 4. lines 7 - 27; Fig. 2.* This is not the same as an input protection circuit including a first lateral bipolar transistor, a second impurity doped region, and a third well region, *wherein said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region* because the base of the first lateral bipolar transistor of the Iwase reference is connected to a

reference voltage and not the second impurity doped region. Accordingly, applicants submit that claim 1, as amended, further distinguishes over the Iwase reference.

The Watt reference does not make up for the deficiencies of the Iwase reference. The Watt reference id directed to an ESD protection structure for a p-well technology. In Fig. 5, an ESD protection structure has been placed between a pad 50 and the V_{ss} 59. A diode 52 is contained in a first p-well and is the negative ESD protection of the ESD protection circuit. The n+ terminal is electrically connected to the pad 50 and the p+ terminal is electrically connected to V_{ss}. The positive ESD protection circuit is contained in p-well 54 which is formed in an n-substrate 56. NMOSFETs have been implemented into p-well 53. The sources 57a and 57b and the gates 57c and 57d are electrically connected to the V_{ss} 59, while the common drain 57e is electrically connected to the pad 50. A resistance 58 is connected between the p-well 53 and the metal conduit of V_{ss} 59. *Col. 7, lines 5 - 25; Fig. 5.*

The Watt reference does not disclose, teach, or suggest the circuit of claim 1, as amended. Unlike the circuit in claim 1, as amended, the Watt reference does not disclose an input protection circuit including an input terminal for supplying an input signal to a circuit to be protected; a semiconductor substrate of a first conductivity type; a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate; first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base; a second well region of the first conductivity type formed in

the principal surface area of said semiconductor substrate; third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate; and a circuit formed in said semiconductor substrate and connected to said input terminal; wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, *said first lateral bipolar transistor operating without a fixed base bias*, and said fourth well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

In contrast, a first lateral bipolar transistor is not included in the Watt reference because there is no first and second impurity doped regions of a first conductivity type to form the first lateral bipolar transistor. Instead, a PN junction diode comprises the negative ESD protection component. *Col. 7, lines 5 - 20; Fig. 5.* Therefore, if a first lateral bipolar transistor is not present in the Watt reference, the first lateral bipolar transistor cannot be operating. Thus, the Watt reference cannot meet the limitation of *said first lateral bipolar transistor operating without a fixed base bias.* Accordingly, Applicants submit that claim 1, as amended, distinguishes over the Watt reference, alone or in combination with, the Iwase reference.

Claim 1, as amended, further distinguishes over the Watt reference. Unlike the circuit of claim 1, as amended, the Watt reference does not disclose an input protection circuit including a second impurity doped region, a first lateral bipolar

transistor, and a third well region, *said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region.*

In contrast, as mentioned above, the Watt reference does not disclose a first lateral bipolar transistor. Thus, the base of the first lateral bipolar transistor cannot be connected to anything since the transistor does not exist. Thus, the Watt reference does not disclose an input protection circuit including a second impurity doped region , a first lateral bipolar transistor, and a third well region, wherein said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region. Accordingly, claim 1, as amended, further distinguishes over the Watt reference, alone or in combination with the Iwase reference.

Claims 2 and 23 - 24, all depend directly on independent claim 1. Accordingly, applicants respectfully submit that dependent claims 2 and 23 - 24, all distinguish over the Iwase and Watt references, alone or in combination, for the reasons set forth above with respect to claim 1.

Independent claim 5, as amended, recites:

> An input protection circuit, comprising:
>
> an input terminal for supplying an input signal to a circuit to be protected;
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> a semiconductor substrate of a first conductivity type;
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> a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;
>
> first and second impurity doped regions of the first conductivity type

formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

second and third well regions of a second conductivity type formed in the principal surface area of said semiconductor substrate, said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor substrate serving as a base;

a circuit formed in said semiconductor substrate and connected to said input terminal;

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region, said first lateral bipolar transistor base operating without a fixed base bias, and said third well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

The Iwase reference does not disclose, teach, or suggest the circuit in claim 5, as amended. Unlike the circuit in claim 5, as amended, the Iwase reference does not disclose an input protection circuit, comprising: an input terminal for supplying an input signal to a circuit to be protected; a semiconductor substrate of a first conductivity type; a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate; first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said

first well region serving as a base; second and third well regions of a second conductivity type formed in the principal surface area of said semiconductor substrate, said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor substrate serving as a base; a circuit formed in said semiconductor substrate and connected to said input terminal; wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region, *said first lateral bipolar transistor base operating without a fixed base bias voltage*, and said third well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

In contrast, the Iwase reference discloses that the first lateral bipolar transistor operates with a fixed base bias because the base of first lateral bipolar transistor, i.e., n^- type well region 16, is supplied with a known constant operating voltage Vpp (e.g., 5 volts). Col. 4, lines 7 - 27 and 50 - 54. This is not the same as an input protection circuit including a first lateral bipolar transistor with a portion of said first well region serving as a base, *said first lateral bipolar transistor operating without a fixed base bias* because the base of the first lateral bipolar transistor of the Iwase reference operates with a fixed base bias. Accordingly, applicants respectfully submit that claim 5, as amended, distinguishes over the Iwase reference.

Claim 5, as amended, further distinguishes over the Iwase reference. Unlike the circuit of claim 5, as amended, the Iwase reference does not disclose an input protection circuit including a second impurity doped region, a first lateral bipolar transistor, and a second well region, *said second impurity doped region and the base of*

said first lateral bipolar transistor are connected to said second well region.

In contrast, the base of said first lateral bipolar transistor in Iwase is connected to a voltage V_{pp} and is not connected to the second impurity doped region or said second well region. *Col. 4, lines 7 - 27; Fig. 2.* This is not the same as an input protection circuit including a first lateral bipolar transistor, a second impurity doped region, and a second well region, *wherein said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region* because the base of the first lateral bipolar transistor of the Iwase reference is connected to a reference voltage and not the second impurity doped region. Accordingly, applicants submit that claim 5, as amended, further distinguishes over the Iwase reference.

The Watt reference does not make up for the deficiencies of the Iwase reference. The Watt reference does not disclose, teach, or suggest the circuit of claim 5, as amended. Unlike the circuit in claim 5, as amended, the Watt reference does not disclose an input protection circuit, comprising: an input terminal for supplying an input signal to a circuit to be protected; a semiconductor substrate of a first conductivity type; a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate; first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base; second and third well regions of a second conductivity type formed in the principal surface area of said semiconductor substrate, said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor

substrate serving as a base; a circuit formed in said semiconductor substrate and connected to said input terminal; wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region, *said first lateral bipolar transistor base operating without a fixed base bias voltage*, and said third well region and the base of the second lateral bipolar transistor are connected to one reference potential node.

In contrast, as discussed above, a first lateral bipolar transistor is not included in the Watt reference. *Col. 7, lines 5 - 20; Fig. 5.* Therefore, if a first lateral bipolar transistor is not present in the Watt reference, the first lateral bipolar transistor cannot be operating. Thus, the Watt reference cannot meet the limitation of *said first lateral bipolar transistor operating without a fixed base bias*. Accordingly, Applicants submit that claim 5, as amended, distinguishes over the Watt reference, alone or in combination with, the Iwase reference.

Claim 5, as amended, further distinguishes over the Watt reference. Unlike the circuit of claim 5, as amended, the Watt reference does not disclose an input protection circuit including a second impurity doped region, a first lateral bipolar transistor, and a second well region, *said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region.*

In contrast, as mentioned above, the Watt reference does not disclose a first lateral bipolar transistor and thus the transistor cannot be connected to anything since the transistor does not exist. Thus, the Watt reference does not disclose an input protection circuit including a second impurity doped region, a first lateral bipolar

transistor, and a second well region, *wherein said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region.* Accordingly, claim 5, as amended, further distinguishes over the Watt reference, alone or in combination with the Iwase reference.

Claims 6 and 25 - 26 all depend directly on independent claim 5. Accordingly, applicants respectfully submit that dependent claims 6 and 25 - 26 all distinguish over the Iwase and Watt references, alone or in combination, for the reasons set forth above with respect to independent claim 5, as amended.

Claim 9 recites:

A semiconductor input protection circuit comprising:

a semiconductor substrate;

a first active region of a first conductivity type defined in said semiconductor substrate;

a second active region of a second conductivity type defined in said semiconductor substrate;

first and second impurity doped regions of the second conductivity type formed in said first active region;

third and fourth impurity dope regions of the first conductivity type formed in said second active region;

an input terminal connected to said first impurity doped region;

a first wiring for connecting said first active region and said second impurity doped region to said third impurity doped region; and

a second wiring for connecting said second active region and said fourth

impurity doped region to a reference potential.

The Bhatia reference does disclose, teach, or suggest the input protection circuit of claim 9. The Bhatia reference is directed to a complimentary field effect transistor structure which eliminates the problems caused by parasitic currents between devices within the structure, i.e., it does not provide input protection for a signal. The circuit of the Bhatia reference is a CMOS FET formed in a semiconductor substrate 2. The p-channel device comprises source 17 and drain 18 regions formed in N type epitaxial layer 6. A n+ type region 14 serves as a contact to layer 6. The N channel transistor is formed in P pocket region 4 and comprises source and drain regions 20 and 21. A p+ type diffusion 23 servers as a contact to the P pocket 4. A guard P+ region 15 and a guard N+ region 22 are formed in a region of the structure between the P and N channel transistors. A VH potential is supplied to region 22 and ground is connected to region 15. Substrate contact 14 is connected to the VH potential and substrate contact 23 is connected to ground. Regions 6, 18, 20, and 4 form a four layer PNPN structure, which acts as a Silicon Controlled Rectifier (SCR). However, because of the guard regions being appropriately biased, the loop gain of the SCR is reduced so it does not latch. This means the currents are contained within the parasistic bipolar devices formed between various regions of the FETs. *Col. 4, line 36 - Col. 5, line 9; Abstract; Fig. 2.*

The Bhatia does not disclose, teach, or suggest the circuit of independent claim 9. The Bhatia reference does not disclose a semiconductor input protection circuit including a semiconductor substrate; a first active region of a first conductivity type defined in said semiconductor substrate; a second active region of a second

conductivity type defined in said semiconductor substrate; first and second impurity doped regions of the second conductivity type formed in said first active region; third and fourth impurity dope regions of the first conductivity type formed in said second active region; *an input terminal connected to said first impurity doped region*; a first wiring for connecting said first active region and said second impurity doped region only to said third impurity doped region; and a second wiring for connecting said second active region and said fourth impurity doped region to a reference potential.

Instead, the Bhatia reference discloses a FET structure that is connected to a voltage potential and ground, where the voltage potential and ground bias the parasitic bipolar devices to eliminate problems caused by parasitic currents between the bipolar devices. *Col. 4, line 36 - Col. 5, line 9.* This is not the same as a semiconductor input protection circuit including an input terminal connected to said first impurity doped region. It also would not have been obvious to replace the input terminal with the voltage potential because they do not serve the same purpose, i.e., the input terminal receives a signal whereas the voltage potential is used to bias the bipolar transistor devices. Therefore, the Bhatia reference does not disclose a semiconductor input protection circuit including an input terminal connected to said first impurity doped region because the input terminal does not exist in the Bhatia reference. Accordingly, applicants respectfully submit that claim 9 distinguishes over the Bhatia reference.

The Iwase reference does not make up for the deficiencies of the Bhatia reference. Unlike the circuit of claim 9, the Iwase reference does not disclose a semiconductor input protection circuit including a semiconductor substrate; a first active region of a first conductivity type defined in said semiconductor substrate; a second

active region of a second conductivity type defined in said semiconductor substrate; first and second impurity doped regions of the second conductivity type formed in said first active region; third and fourth impurity dope regions of the first conductivity type formed in said second active region; an input terminal connected to said first impurity doped region; *a first wiring for connecting said first active region and said second impurity doped region to said third impurity doped region*; and a second wiring for connecting said second active region and said fourth impurity doped region to a reference potential.

Instead, the Iwase reference discloses a wiring connecting a first active region to a voltage V_{PP}, but not to a second impurity doped region. *Col. 4, line 18 - 27.* This is not the same as a semiconductor input protection circuit including a first wiring for connecting said first active region and said second impurity doped region to said third impurity doped region because the first active region is not connected to the second impurity doped region. Accordingly, applicants respectfully submit that claim 9, distinguishes over the Iwase reference, alone or in combination with, the Bhatia reference.

The Watt reference does not make up for the deficiencies of the Bhatia and Iwase references. Unlike the circuit of claim 9, the Watt reference does not disclose a semiconductor input protection circuit including a semiconductor substrate; a first active region of a first conductivity type defined in said semiconductor substrate; a second active region of a second conductivity type defined in said semiconductor substrate; first and second impurity doped regions of the second conductivity type formed in said first active region; third and fourth impurity dope regions of the first conductivity type formed

in said second active region; an input terminal connected to said first impurity doped region; *a first wiring for connecting said first active region and said second impurity doped region to said third impurity doped region*; and a second wiring for connecting said second active region and said fourth impurity doped region to a reference potential.

Instead, the Watt reference discloses a wiring connecting an input pad to a second impurity doped region, but not the connecting of the second impurity doped region to a first active region. *Col. 7, lines 5 - 25; Fig. 5.* This is not the same as a semiconductor input protection circuit including a first wiring for connecting said first active region and said second impurity doped region to said third impurity doped region because the second impurity doped region is not connected to the first active region. Accordingly, applicants respectfully submit that claim 9, as amended, distinguishes over the Watt reference, alone or in combination with, the Bhatia and the Iwase references.

Further, there is no motivation to combine the Bhatia, Iwase, and Watt references. The Bhatia reference is directed to a structure that is designed to contain parasitic currents of parasitic bipolar devices, i.e., transistors, which reside within the structure. The Bhatia reference does not teach the receiving of an input signal to a circuit that is to be protected, instead it only discloses receiving a voltage and a ground that appropriately bias the parasitic bipolar devices and guard regions. The Iwase reference is directed to providing protection to an input terminal supplied input signal that is received by a CMOS inverter. The Watt reference is directed to providing ESD protection for input, output, and I/O pins. The providing of protection against problems caused by parasitic currents between bipolar devices is not the same field as providing

input protection, e.g., ESD protection, for a signal input via an input terminal and output to a circuit or a pin. Thus, a person of ordinary skill in the art would not have been motivated to look at references discussing solutions to parasitic currents between bipolar devices in a semiconductor when attempting to find a solution for providing input protection to an input signal that is to be supplied to a circuit or to a pin. Therefore, the Bhatia, Iwase, and Watt references are not properly combinable with respect to the present invention.

Claims 10, 12, and 14 - 19, depend, directly or indirectly, from claim 9. Accordingly, applicants respectfully submit that dependent claims 10, 12, and 14 - 19, all distinguish over the Bhatia, Iwase, and Watt references, alone or in combination, for the reasons set forth above with respect to independent claim 9, as amended.

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Applicants believe that the foregoing amendments place the application in condition for allowance, and a favorable action is respectfully requested. If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call either of the undersigned attorneys at the Los Angeles telephone number (213) 488-7100 to discuss the steps necessary for placing the application in condition for allowance should the Examiner believe that such a telephone conference would advance prosecution of the application.

Respectfully submitted,

Date: May 5, 2003

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APPENDIX
VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Please cancel claims 3, 4, 7, 8, 11, 13, 20, 21, and 22, without prejudice. Please amend claims 1 and 5. Please add claims 23 - 26.

1. (Twice Amended) An input protection circuit [according to claim 21,] comprising:

an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

a second well region of the first conductivity type formed in the principal surface area of said semiconductor substrate;

third and fourth well regions of the second conductivity type formed in said second well region and forming a second lateral bipolar transistor with a portion of said second well region serving as a base, bottoms of said third and fourth well regions forming a PN junction with said second well or with said semiconductor substrate; and

a circuit formed in said semiconductor substrate and connected to said

input terminal;

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said third well region, said first lateral bipolar transistor operating without a fixed base bias, and said fourth well region and the base of the second lateral bipolar transistor are connected to [said] one reference potential node.

5. (Twice Amended) An input protection circuit, [according to claim 22,] comprising:

an input terminal for supplying an input signal to a circuit to be protected;

a semiconductor substrate of a first conductivity type;

a first well region of a second conductivity type opposite to the first conductivity type, said first well region being formed in one principal surface area of said semiconductor substrate and forming a PN junction with said semiconductor substrate;

first and second impurity doped regions of the first conductivity type formed in said first well region and forming a first lateral bipolar transistor with a portion of said first well region serving as a base;

second and third well regions of a second conductivity type formed in the principal surface area of said semiconductor substrate, said second and third well regions forming a second lateral bipolar transistor with a portion of said semiconductor substrate serving as a base;

a circuit formed in said semiconductor substrate and connected to said input terminal;

wherein said input terminal is connected to said first impurity doped region, said second impurity doped region and the base of said first lateral bipolar transistor are connected to said second well region, said first lateral bipolar transistor operating without a fixed base bias, and said third well region and the base of the second lateral bipolar transistor are connected to [said] one reference potential node.

23. (New) The input protection circuit of claim 1, wherein the second lateral bipolar transistor is turned on to protect the input protection circuit when a high voltage of a first polarity, the first polarity corresponding to the first conductivity type, is applied to the input terminal.

24. (New) The input protection circuit of claim 1, wherein the first lateral bipolar transistor is turned on to protect the input protection circuit when a high voltage of a second polarity, the second polarity corresponding to the second conductivity type, is applied to the input terminal.

25. (New) The input protection circuit of claim 5, wherein the second lateral bipolar transistor is turned on to protect the input protection circuit when a high voltage of a first polarity, the first polarity corresponding to the first conductivity type, is applied to the input terminal.

26. (New) The input protection circuit of claim 5, wherein the first lateral bipolar transistor is turned on to protect the input protection circuit when a high voltage of a second polarity, the second polarity corresponding to the second conductivity type, is applied to the input terminal.